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Efficient Structure for Testing Operational Amplifiers

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Abstract

Rapid advances in application specific integrated circuits have posed a challenge in both design and test of analog components to provide consistent circuit performance. In this paper, a structure is proposed and designed that will help the ASIC industries in testing analog components. The Op-Amp under test is configured as voltage follower and the signature is analyzed using digital circuitry.

Keywords: OA,

Introduction

Integration of more and more functionality onto silicon by designers results in the increase of test cost [1]. Statistical analysis can be used to reduce test time and test cost of analog and mixed signal ICs [2-5]. Research conducted on fault based testing had shown that the failures arise from physical faults which can be detected by simpler tests. Fault based testing can be classified into three types:

- Static DC testing
- Steady state AC testing
- Dynamic Transient Testing

In static DC testing, faults like open, short and bridging faults is measured based on node voltages and branch currents [6] but, the minus side is that it cannot be used to detect parameter variations. AC testing can measure parametric faults but it is too expensive as the measurements should be made under steady state conditions [7]. In transient testing, the response is sampled at specified time points for fault detection [8]. Hence, it necessitates developing an efficient technique to test operational amplifier circuits as they are the major building blocks in any analog and mixed signal circuits.

In this paper, a structure is proposed for testing amplifiers. The test strategy, simulation results are presented in the following sections respectively.

The Proposed Approach and Test Strategy

Transition counting technique finds the number of 0 to 1 and 1 to 0 transitions [9]. Instead of determining both transitions, detect 1 to 0 transitions alone in a given time window. The strategy employed is based on the high frequency and time domain parameter deviation, slew rate. The slew rate is measured from the slope of the transient response. The presence of a fault deviate the slew rate of the opamp [10-11].

The time domain metric slew rate can be measured by digital circuitry. This is shown in Figure1. The output of the inverter is sampled at the two instances T1 and T2 using D-latches. This timing window is shown in Figure 3. The output of D-latches results in a pair of values V1 and V2. Logically, for a fault free opamp the value is (1, 0) and (1, 1) or (0, 0) for faulty ones. Thus the output of digital circuitry represents the signature which is used to study the opamp under test.

Structure

The proposed scheme is shown in Figure 1. The test signal T activates the circuit. The delay elements are implemented using NAND gates. Both delay elements and combinational logic are used to generate the control signals C1, C2, C3 and C4.These control signals are not shown in Figure 2. These control signals generate clock signal CK, which are used to clock the flip-flops F1 and F2. The waveforms are shown in Figure 3. This combination of flip-flops generates output signatures, which is used to detect whether the opamp is faulty or not.

Operation

The time reference is the instant when the signal T goes high. During the first timing window, the output of the inverter is latched into F2, giving the first value V2. During the second timing window, the value of V2 is transferred to F1, giving the value V1.Thus the pair of values (V1, V2) represents the

signature of the opamp under test, which must be (1, 0) for a fault free opamp.

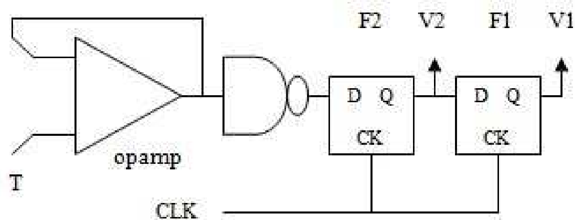

Figure 1 Proposed scheme

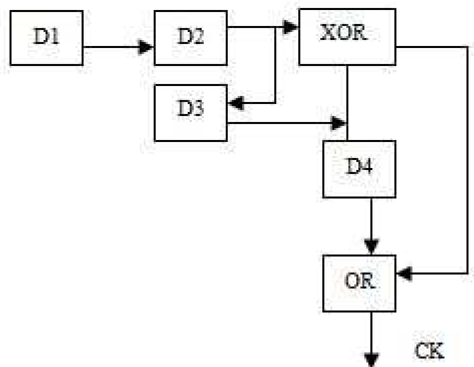

Figure 2 Control and clock signal generation

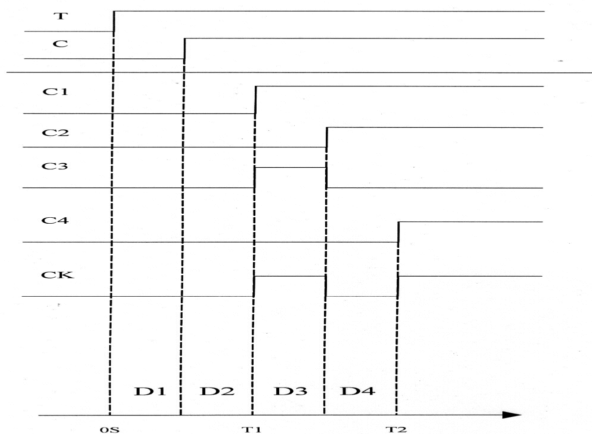

Figure 3 Waveforms of control signals and clock

Simulation Results

For simulation purpose, consider a set of hard faults. The hard faults are classified as short faults; (a) gate to drain short (b) gate to source and (c) drain to source shorts and open faults, (a) gate open (b) drain open and (c) source open faults. Gate to source faults is studied and modelled by a small resistance between the shorted terminals according to [11]. Figure 4 shows the simulation results for the case of gate to source short fault. From the results shown in Figure 4 M1 and M2 corresponds to the clock signal. During the first timing window, the fault was not detected while for the second window fault was detected and the signature is equal to (0, 1).

The gate to source short fault coverage is 100% but the overall fault coverage considering all fault types is only 32%.

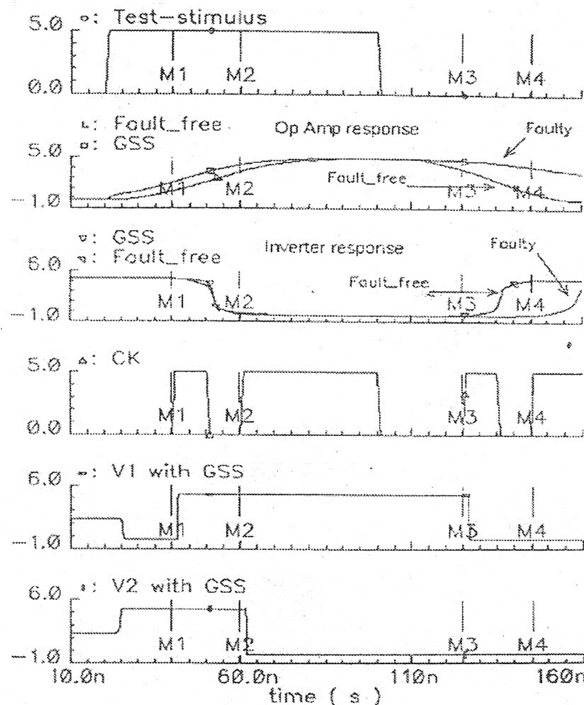

Figure 4 Results of gate to source short fault

Conclusions

This paper had presented a structure that can simplify the test stimulus generation and reduce test time with negligible impact on circuit performance thus fulfilling the growing needs of ASIC industries. The gate to source short fault coverage is 100%.

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